

FIG. 1A

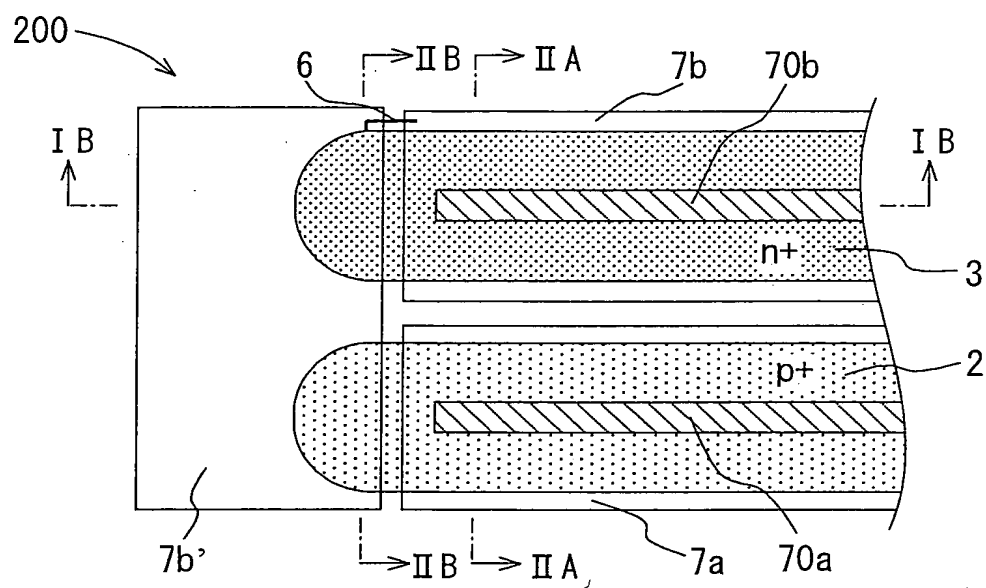


FIG. 1B

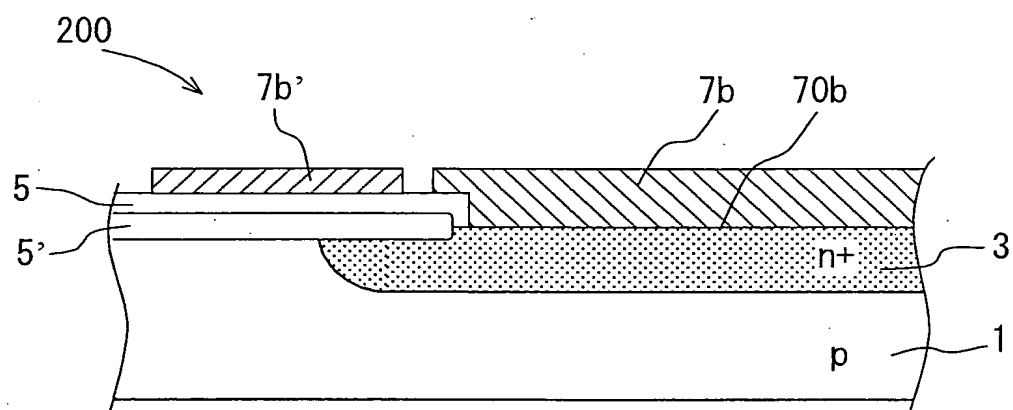


FIG. 2A

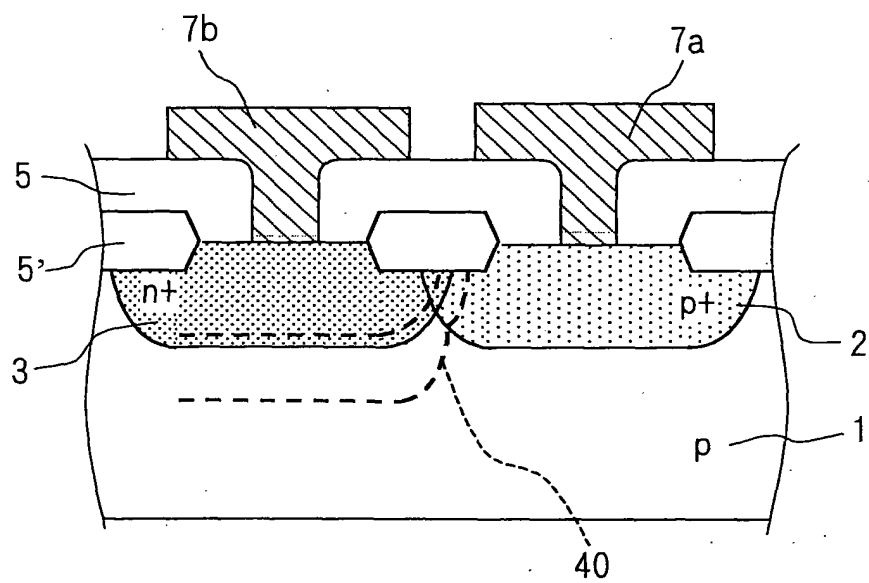


FIG. 2B

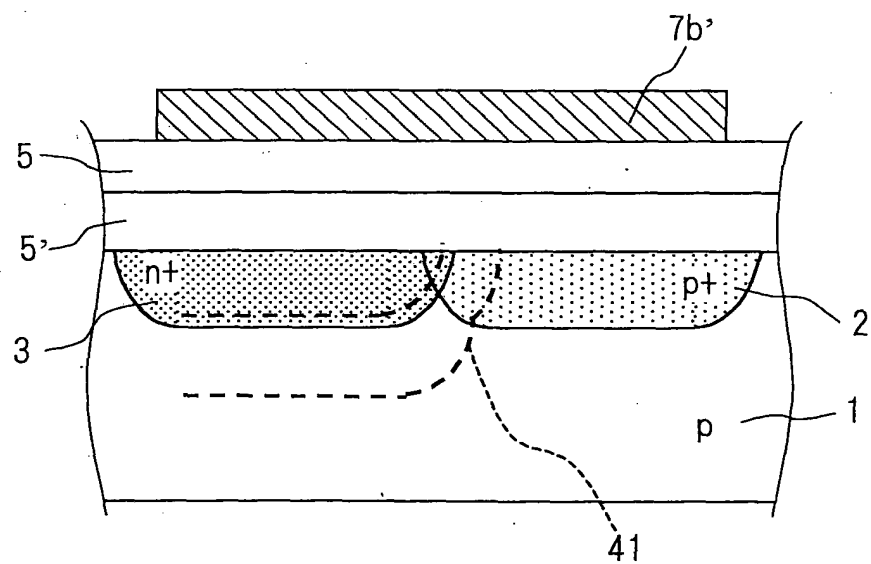


FIG. 3A

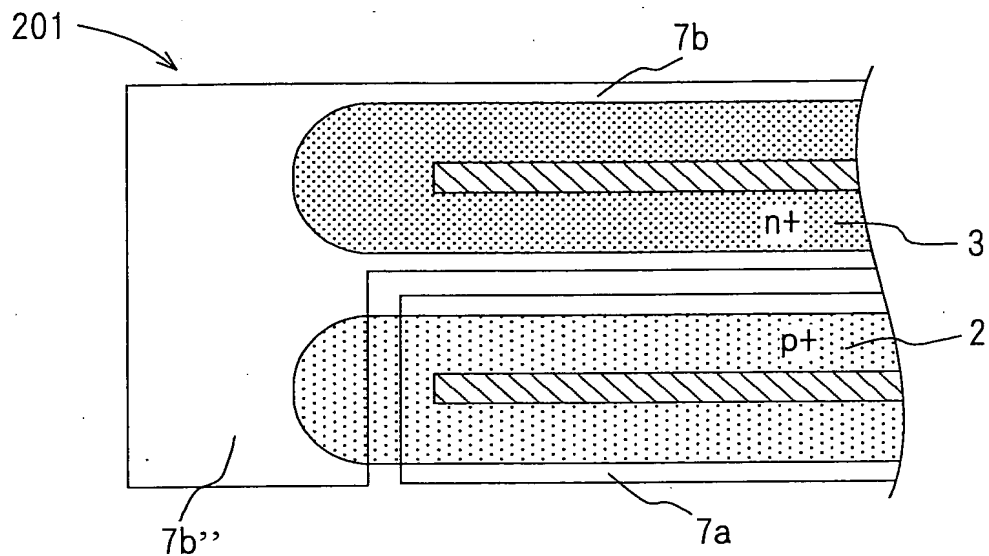


FIG. 3B

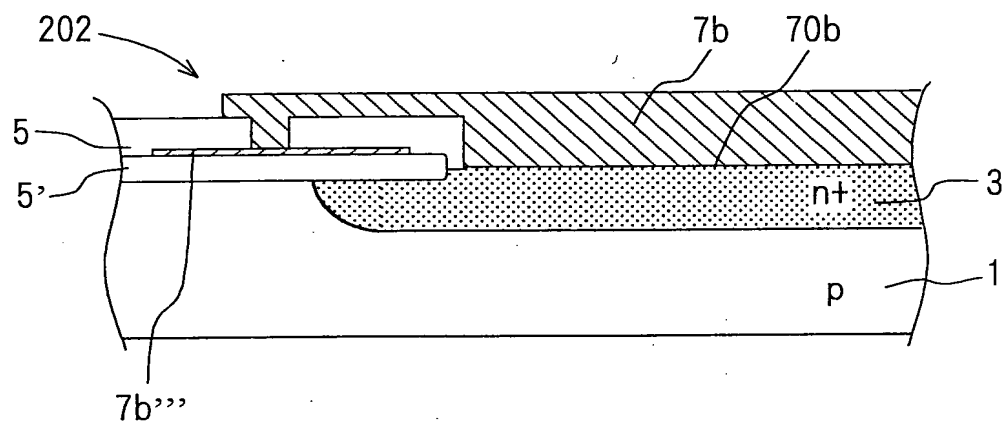


FIG. 4

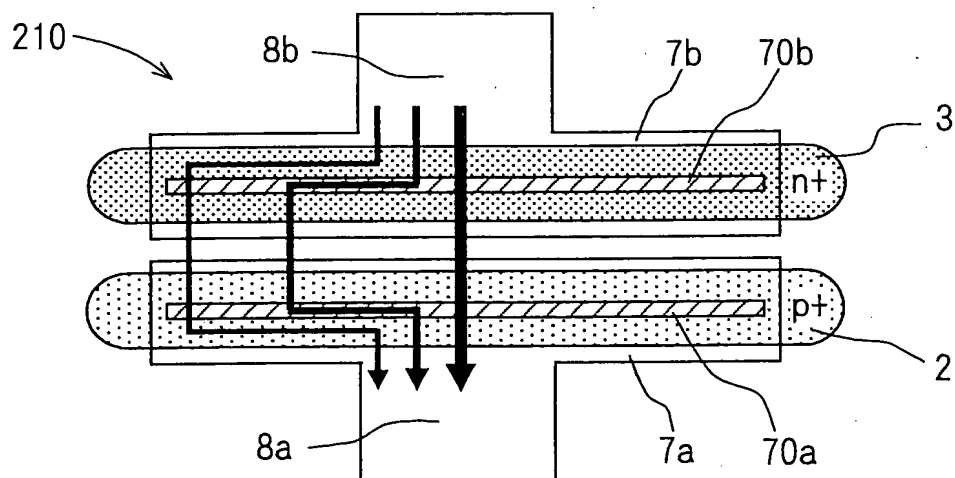


FIG. 5

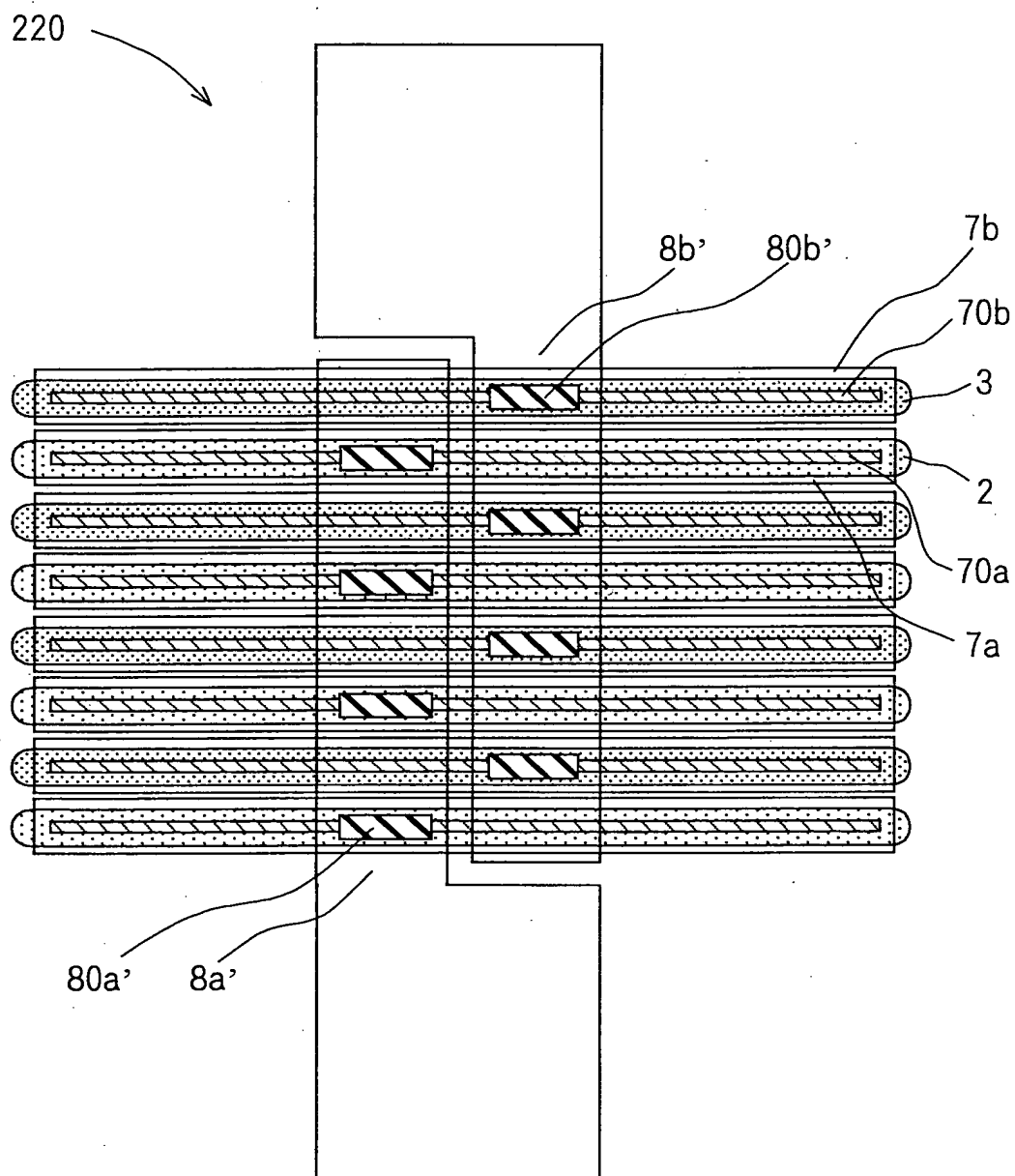


FIG. 6

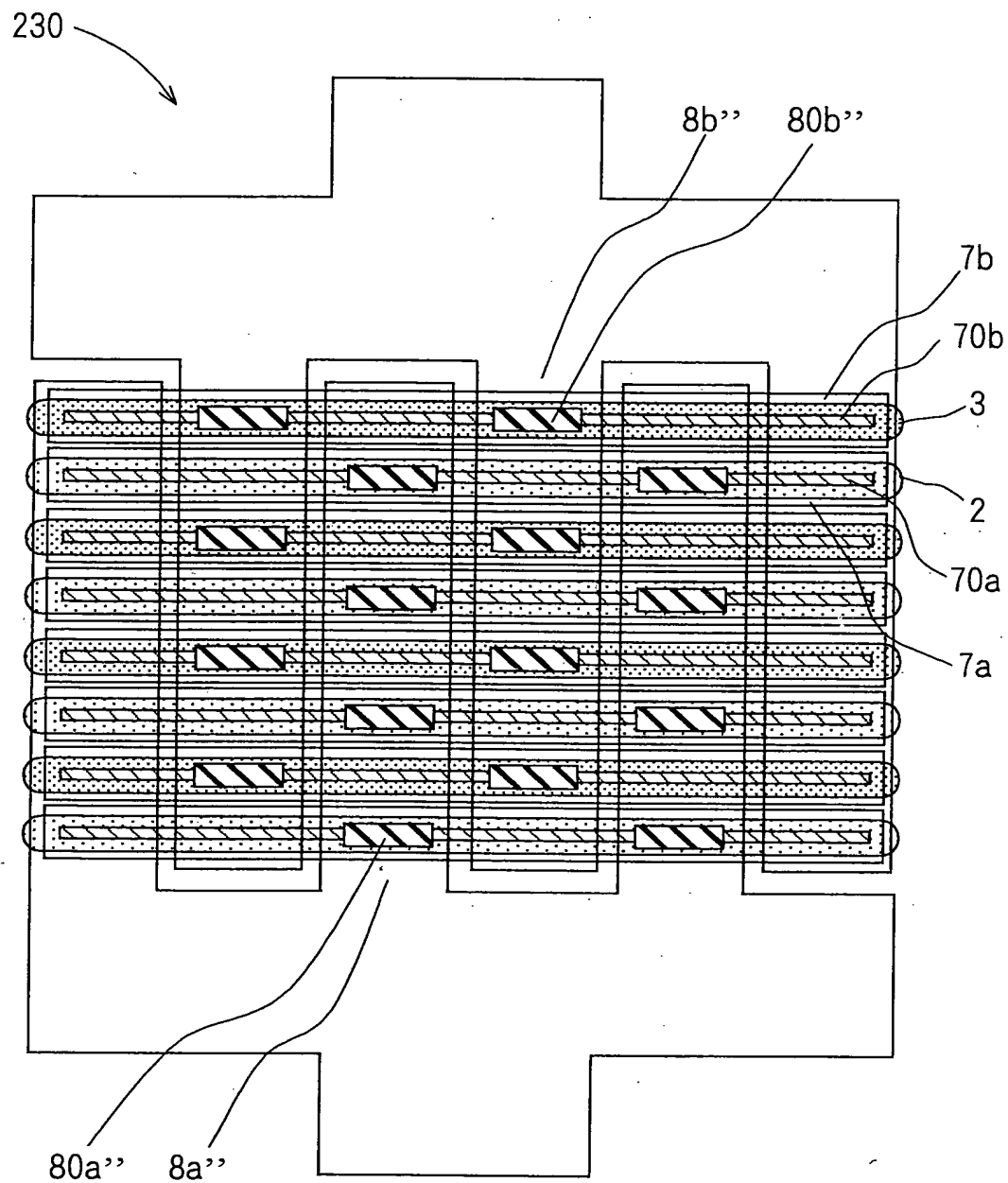


FIG. 7A

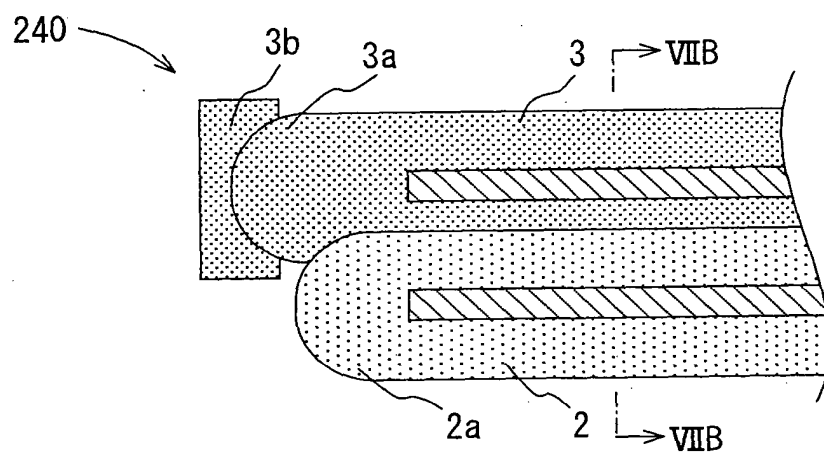


FIG. 7B

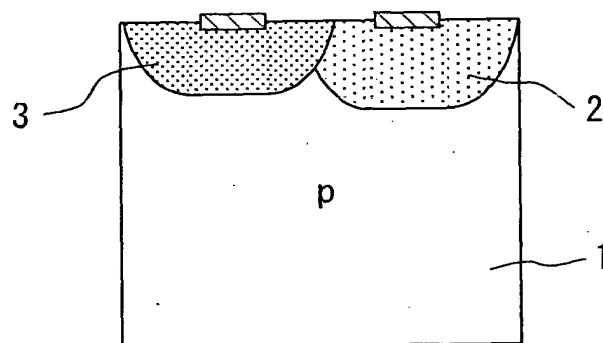


FIG. 8

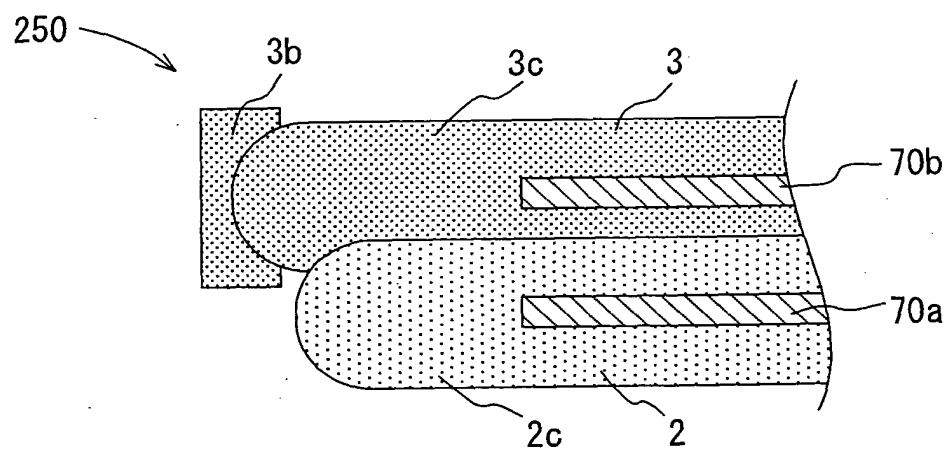


FIG. 9A

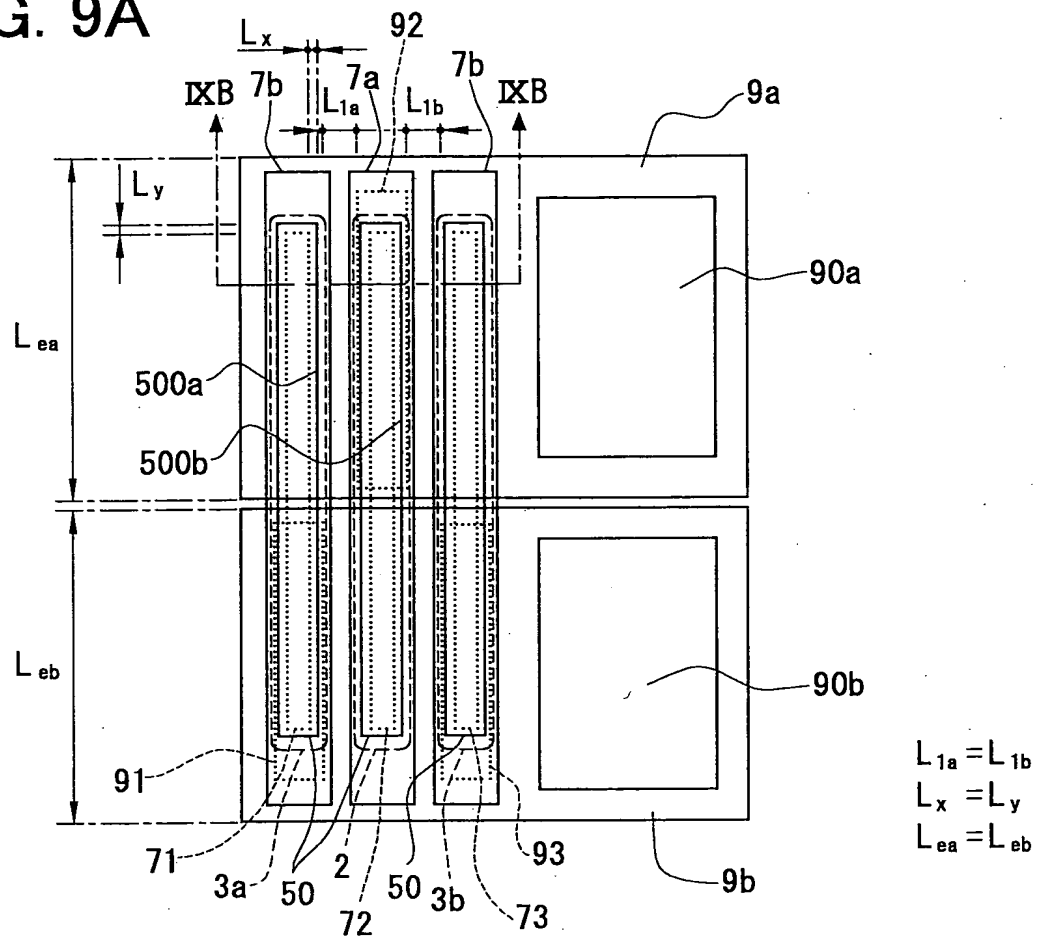


FIG. 9B

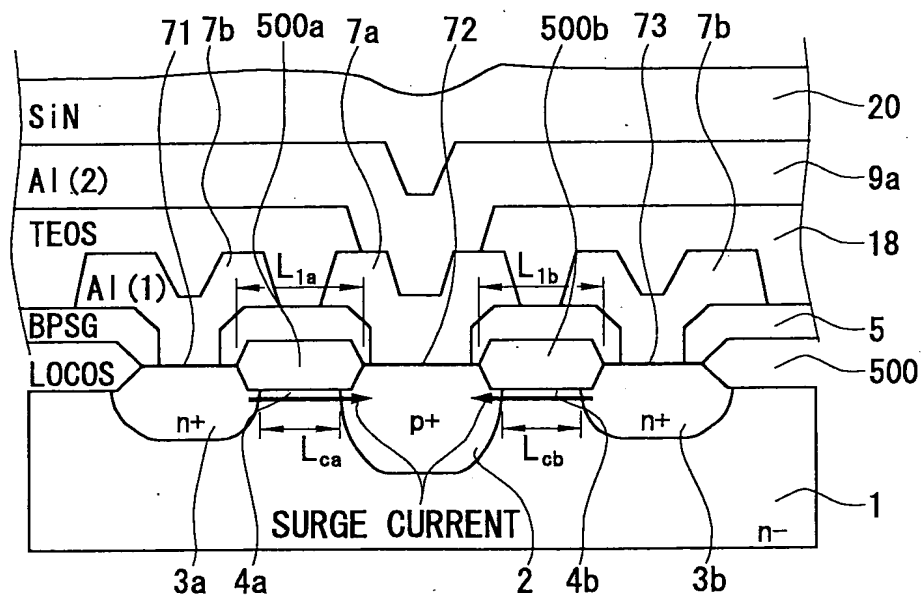


FIG. 10A

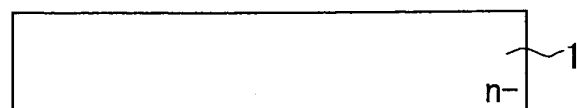


FIG. 10B

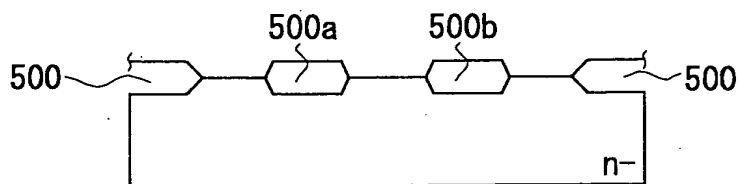


FIG. 10C

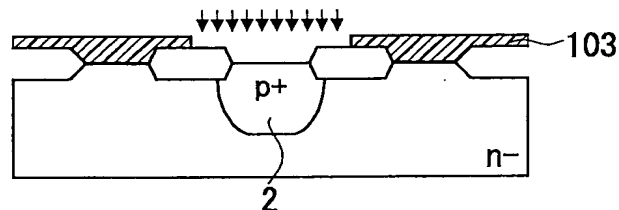


FIG. 10D

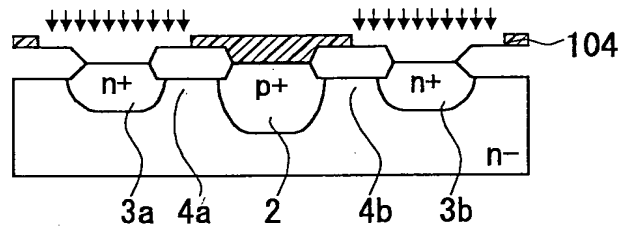


FIG. 10E

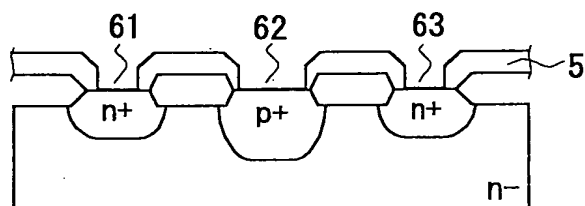


FIG. 10F

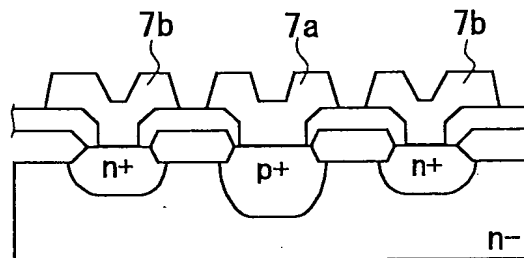


FIG. 10G

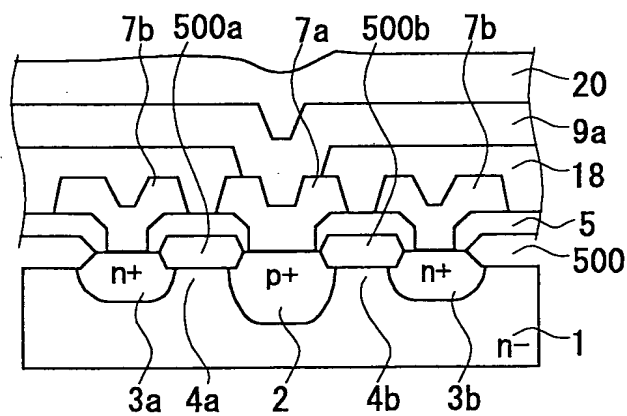


FIG. 11A

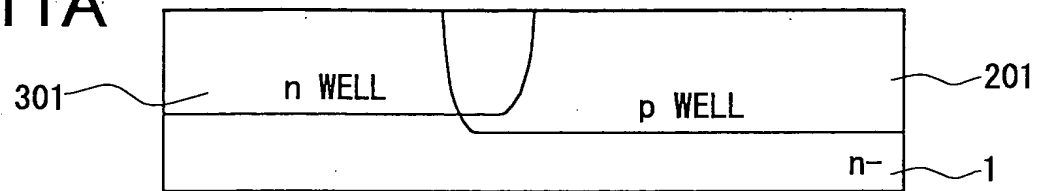


FIG. 11B

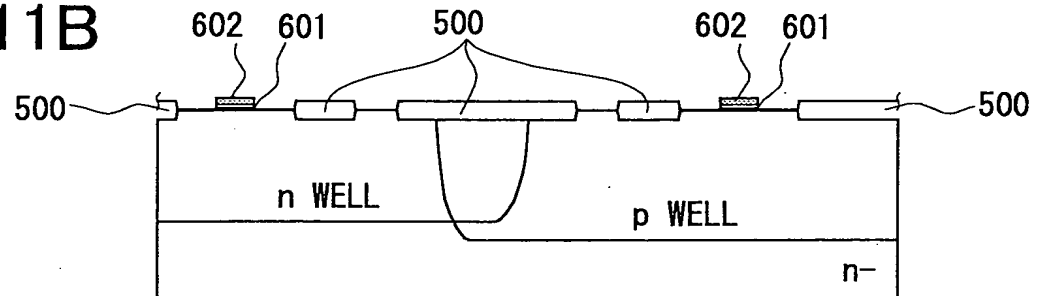


FIG. 11C

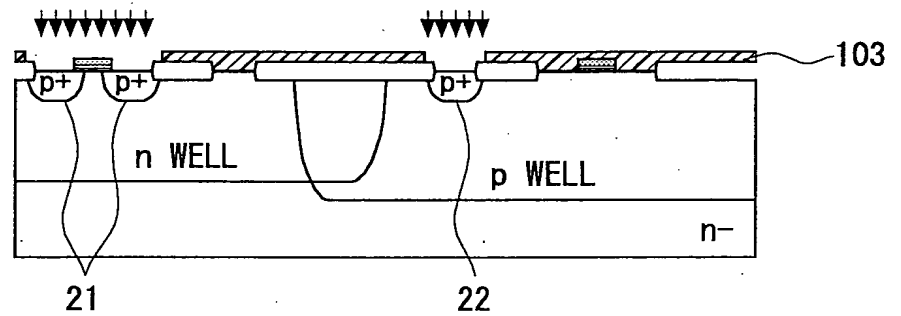


FIG. 11D

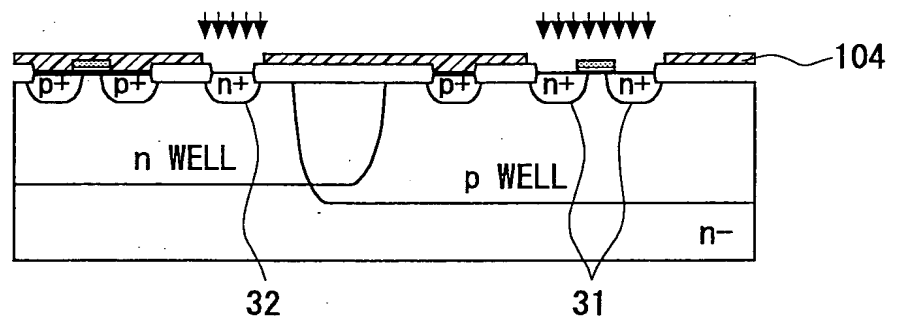


FIG. 11E

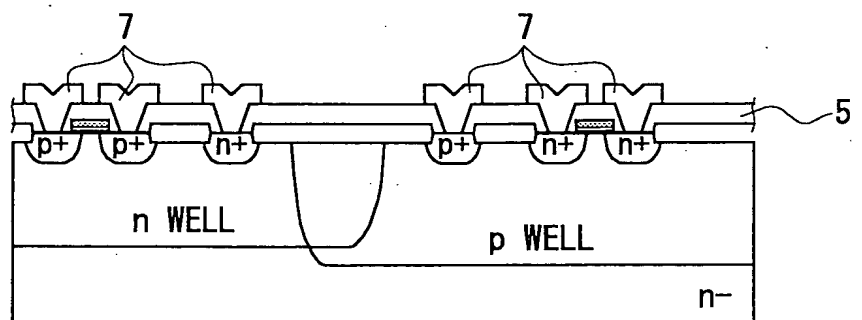


FIG. 12

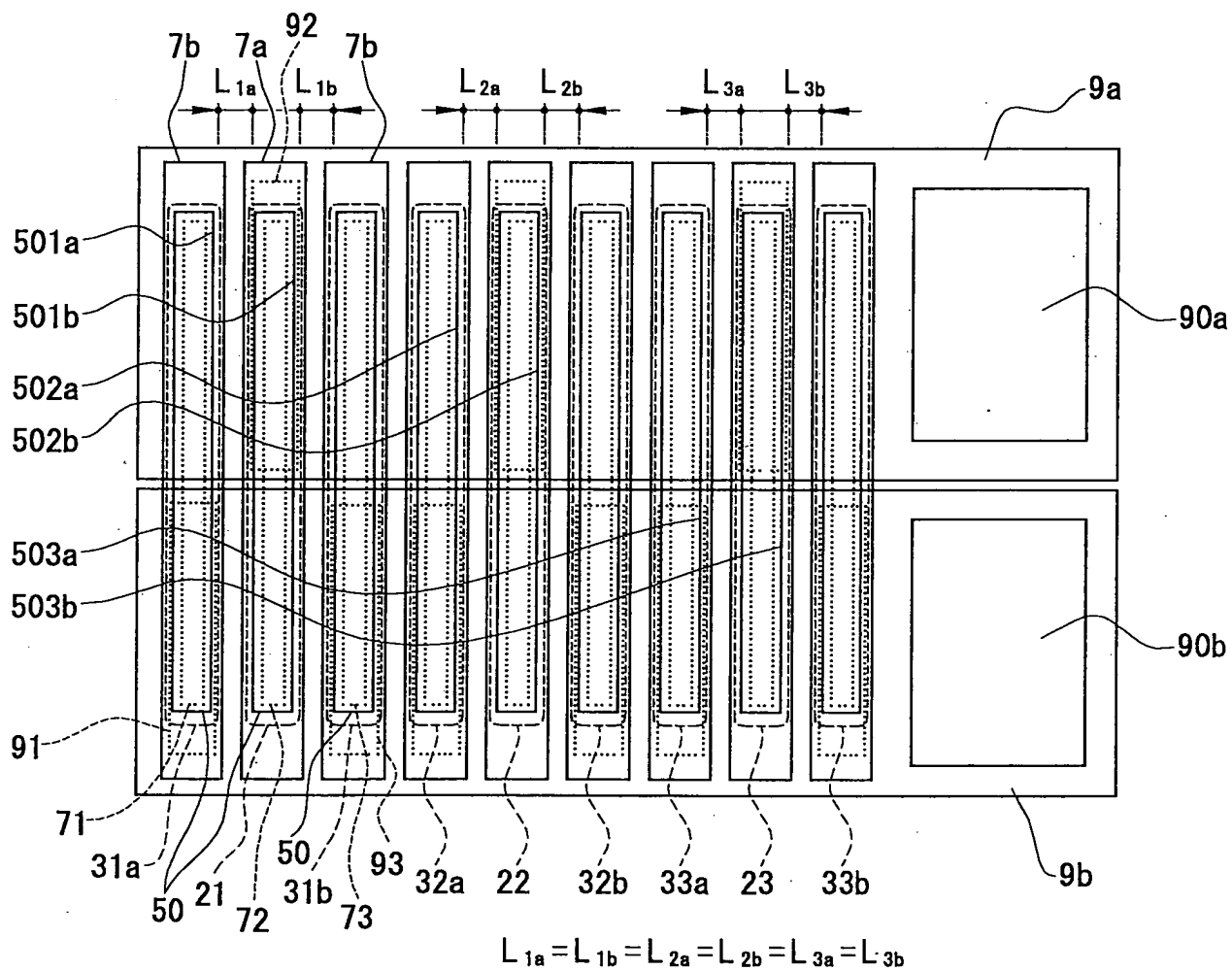


FIG. 13

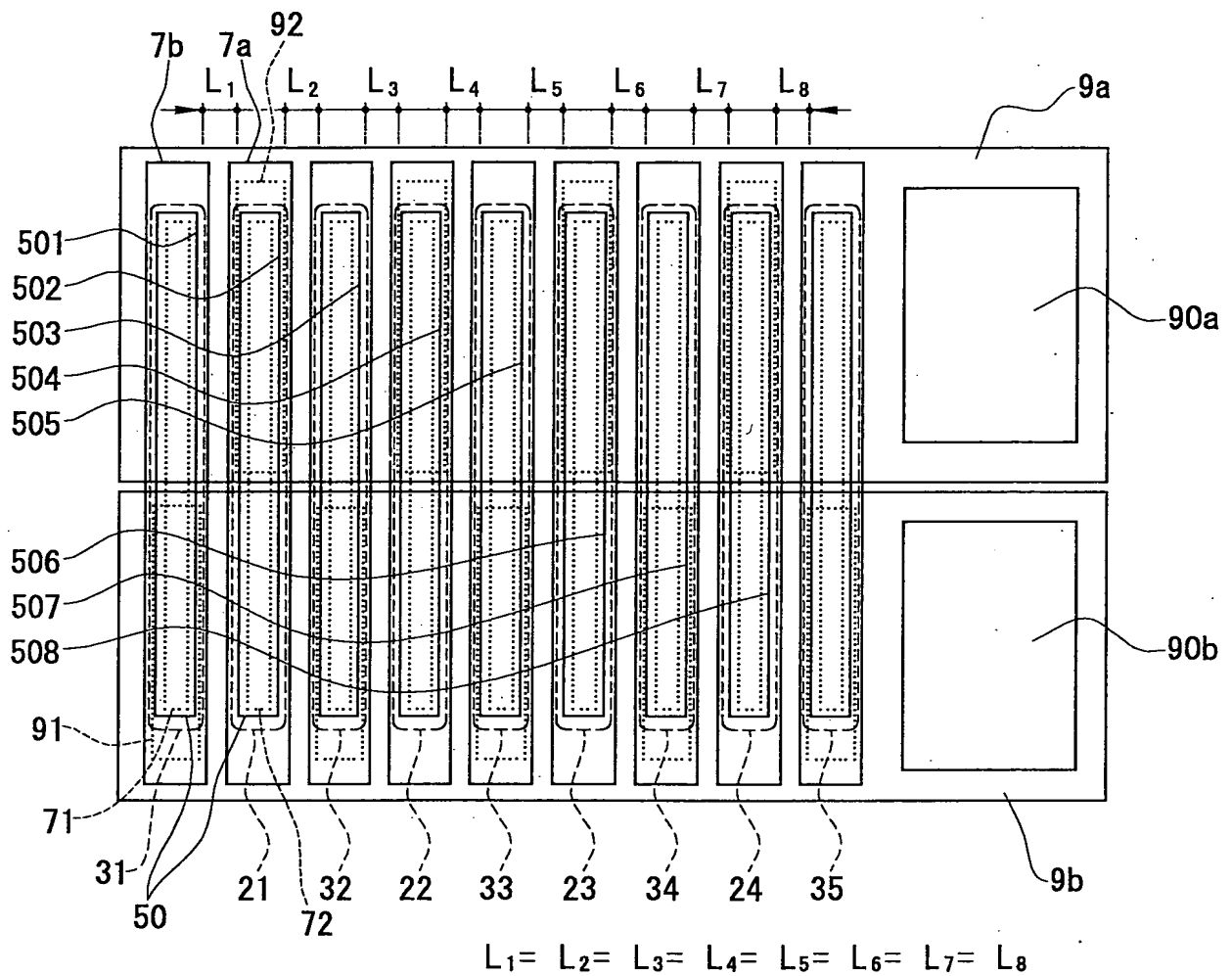


FIG. 14

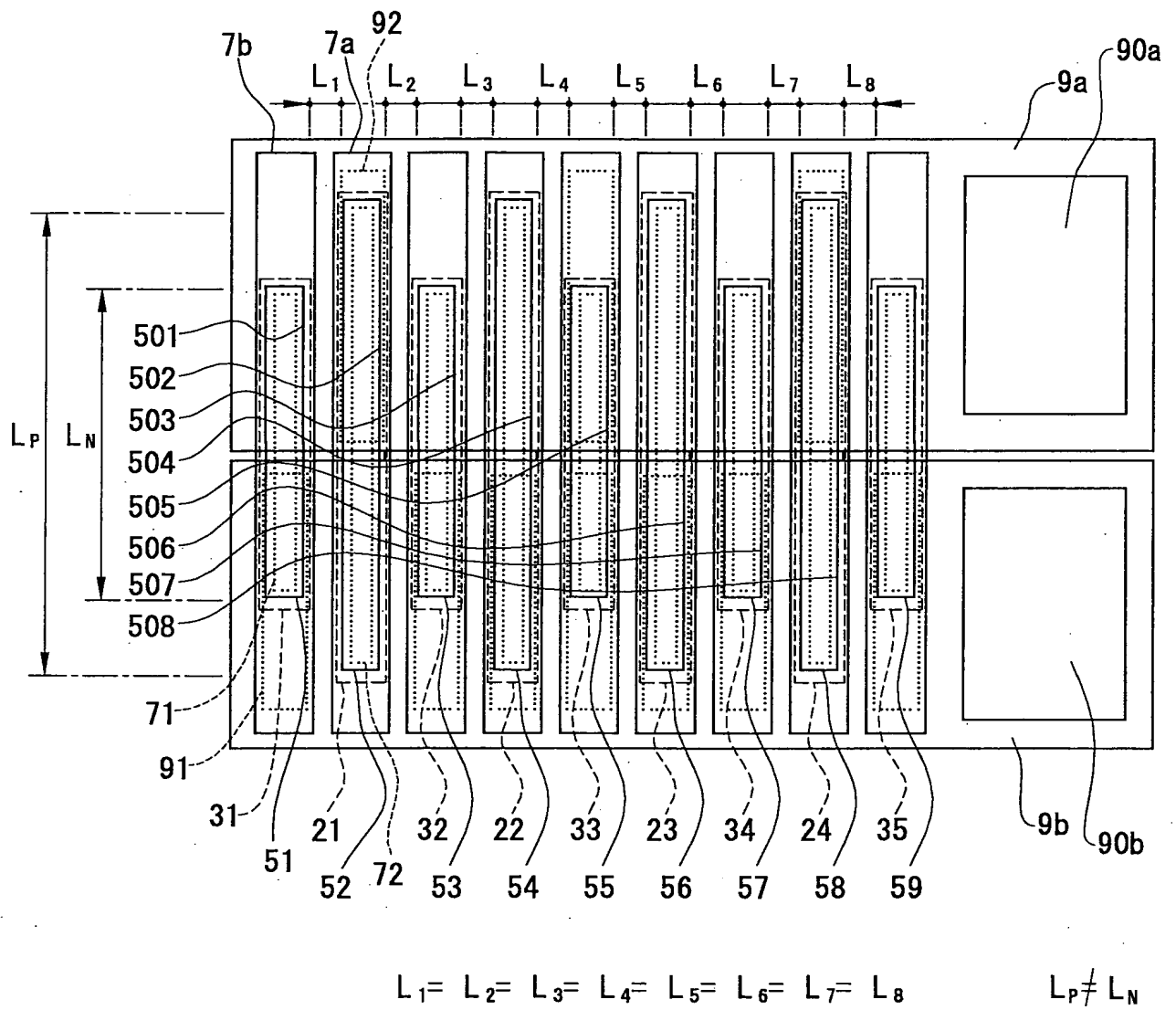
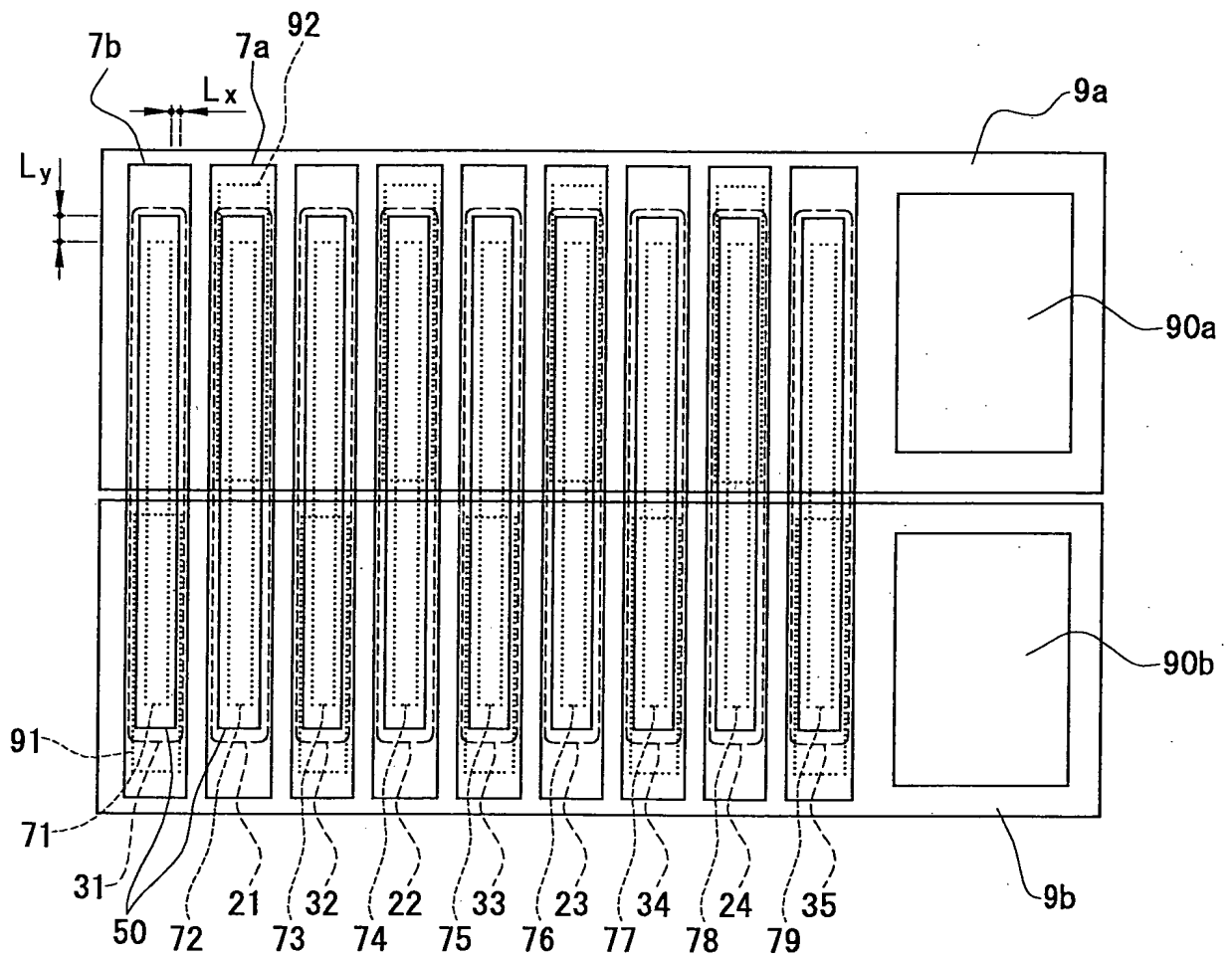


FIG. 15



[illegible]

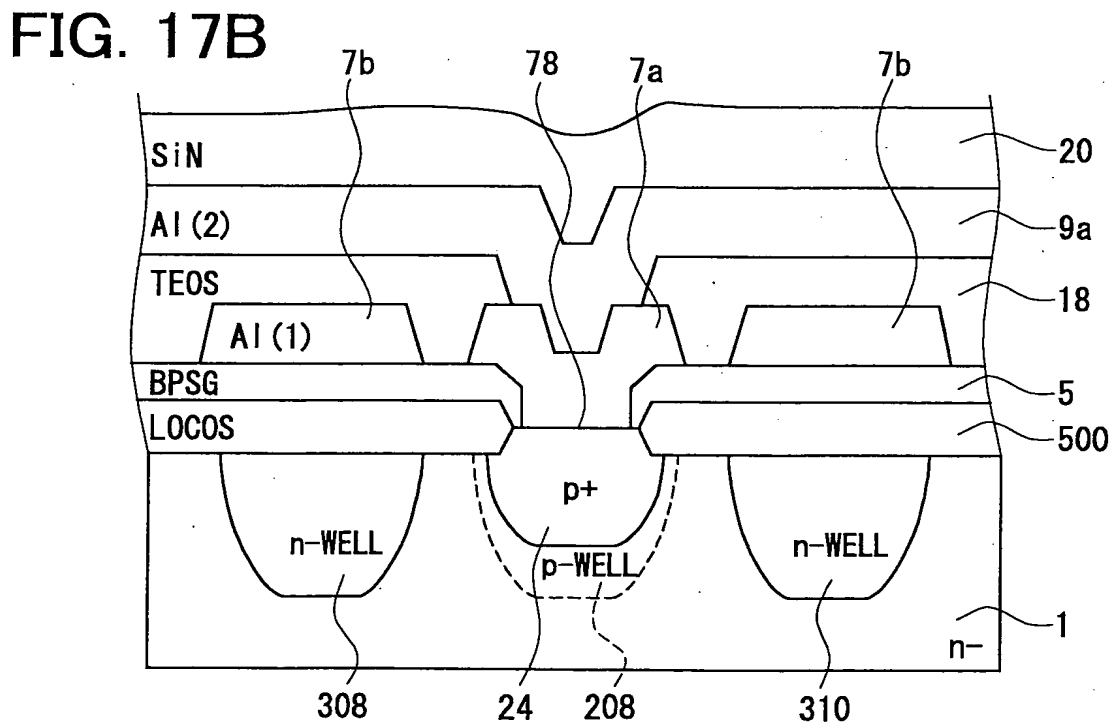
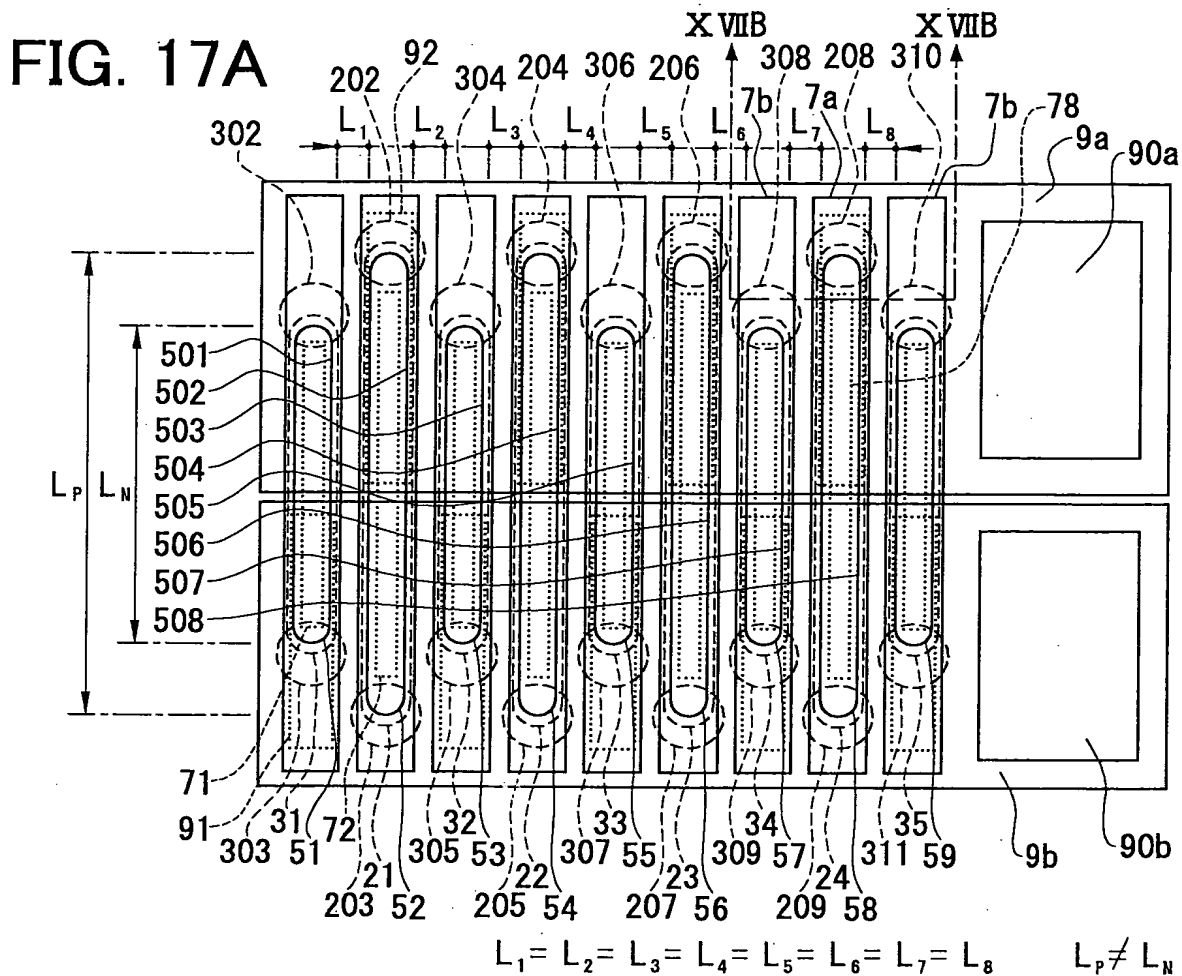


FIG. 18

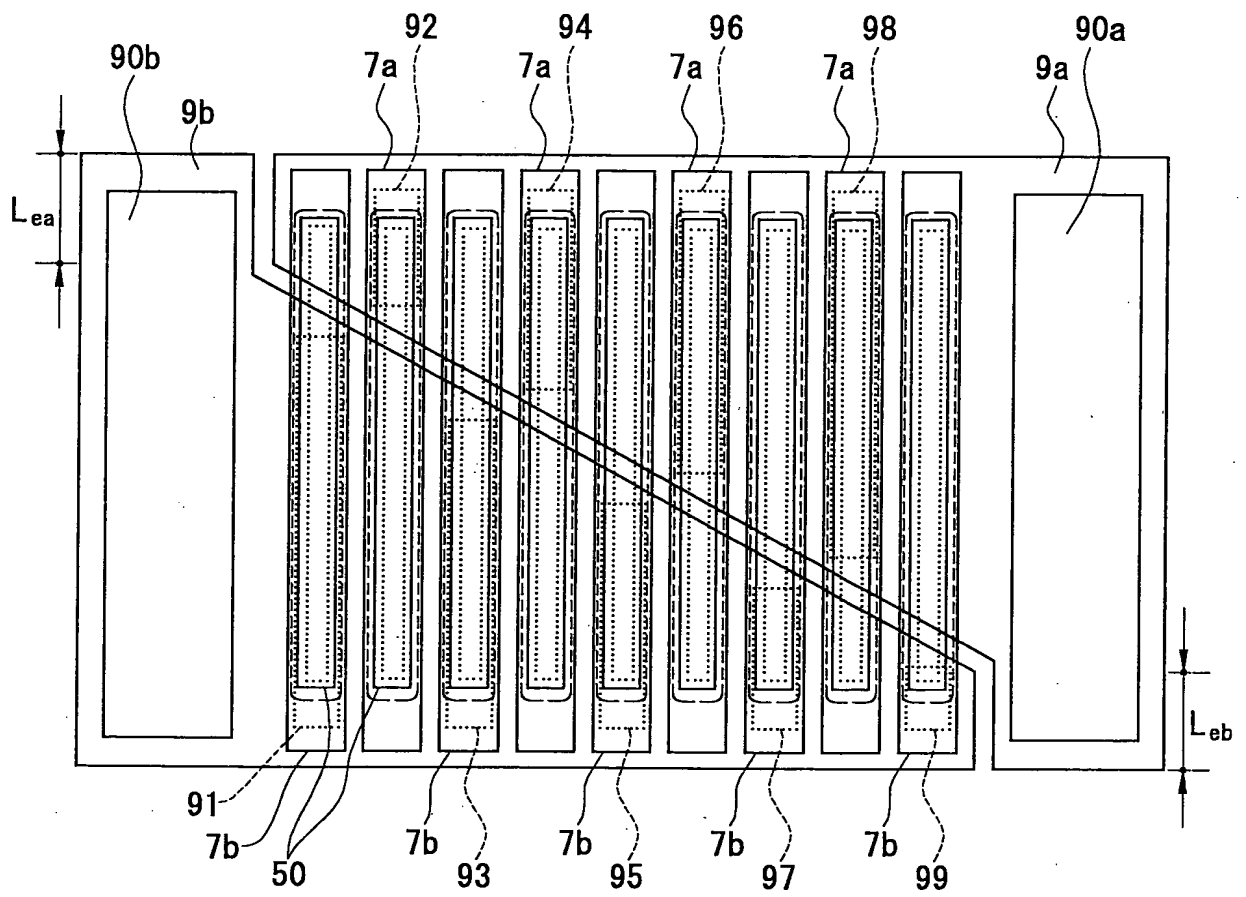


FIG. 19A

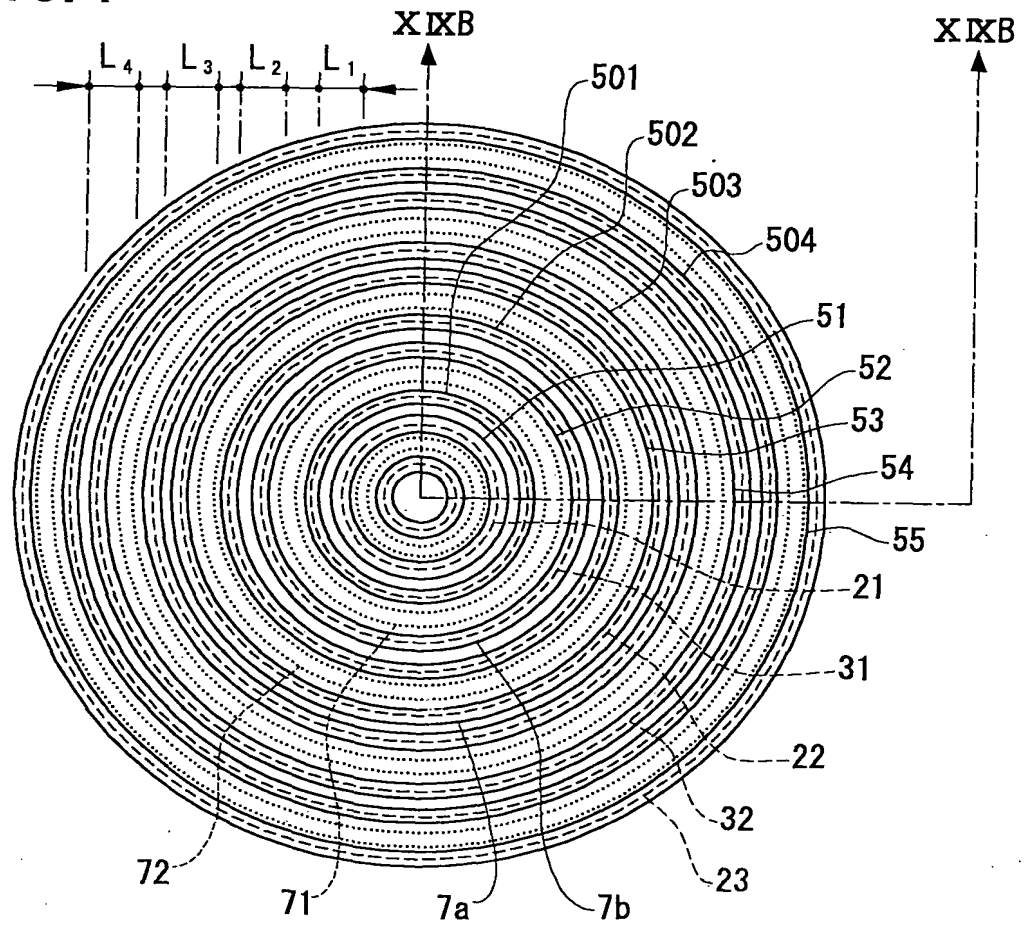


FIG. 19B

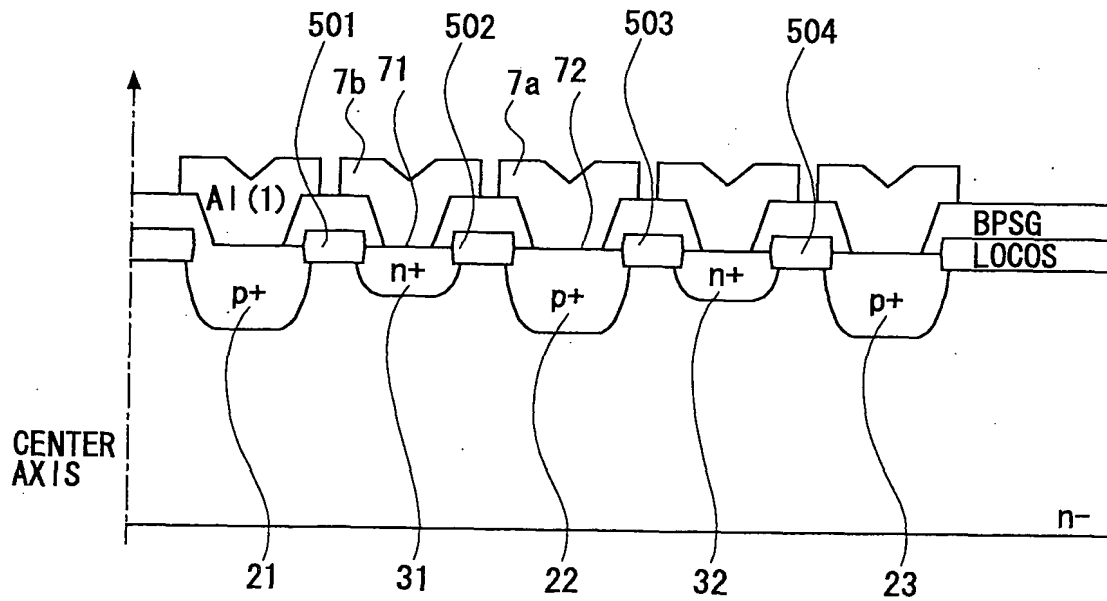


FIG. 20A

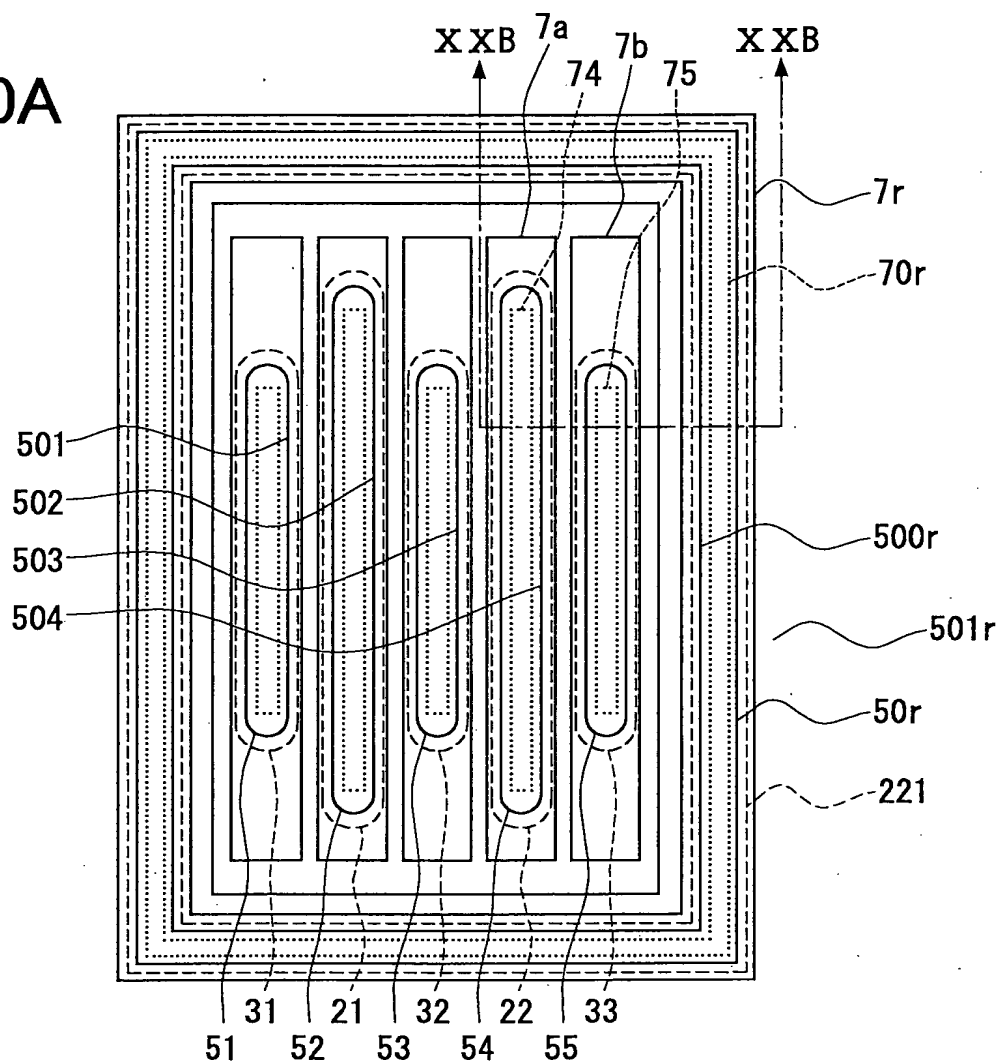


FIG. 20B

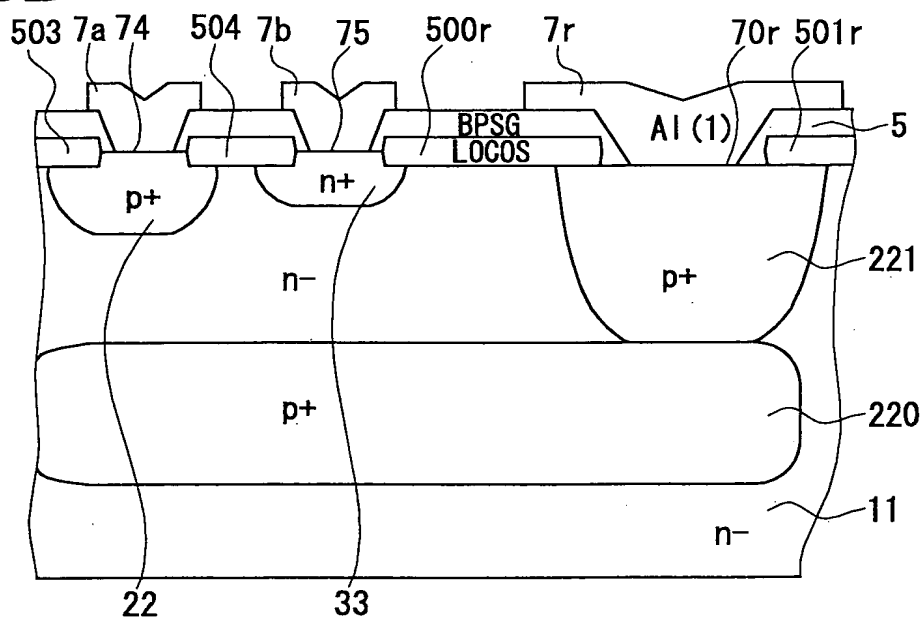


FIG. 21A

FIG. 21A is a schematic diagram of a device 700. The device 700 is shown in cross-section, revealing a substrate 401. Within the substrate 401, there are five vertical channels or regions labeled 51, 52, 53, 54, and 55. Each of these regions contains a central core element: 31 in 51, 21 in 52, 32 in 53, 22 in 54, and 33 in 55. These core elements are surrounded by a dashed outline 74 and an outer layer 75. The entire assembly is enclosed within a frame or housing 700. Section lines XX I B are indicated at the top of the diagram, with arrows pointing to the right.

This cross-sectional view illustrates a semiconductor device. The top layer consists of a gate stack with a BPSG (Boron Phosphorus Silicate Glass) layer (503) and a LOCOS (Local Oxidation of Silicon) layer (74). Below the gate stack, there is a polysilicon gate (POLY Si, 75) and a p-n junction structure. The p-n junction is formed by a p+ region (22) and an n+ region (33). The device is surrounded by a SiO2 layer (401) and a POLY Si layer (700). The bottom layer is a SiO2 layer (402) on top of an n- substrate (11). Other labels include 504, 7b, 75, 500r, BPSG, LOCOS, p+, n+, SiO2, POLY Si, n-, 11, 401, 700, 402, 22, and 33.

FIG. 22A
RELATED ART

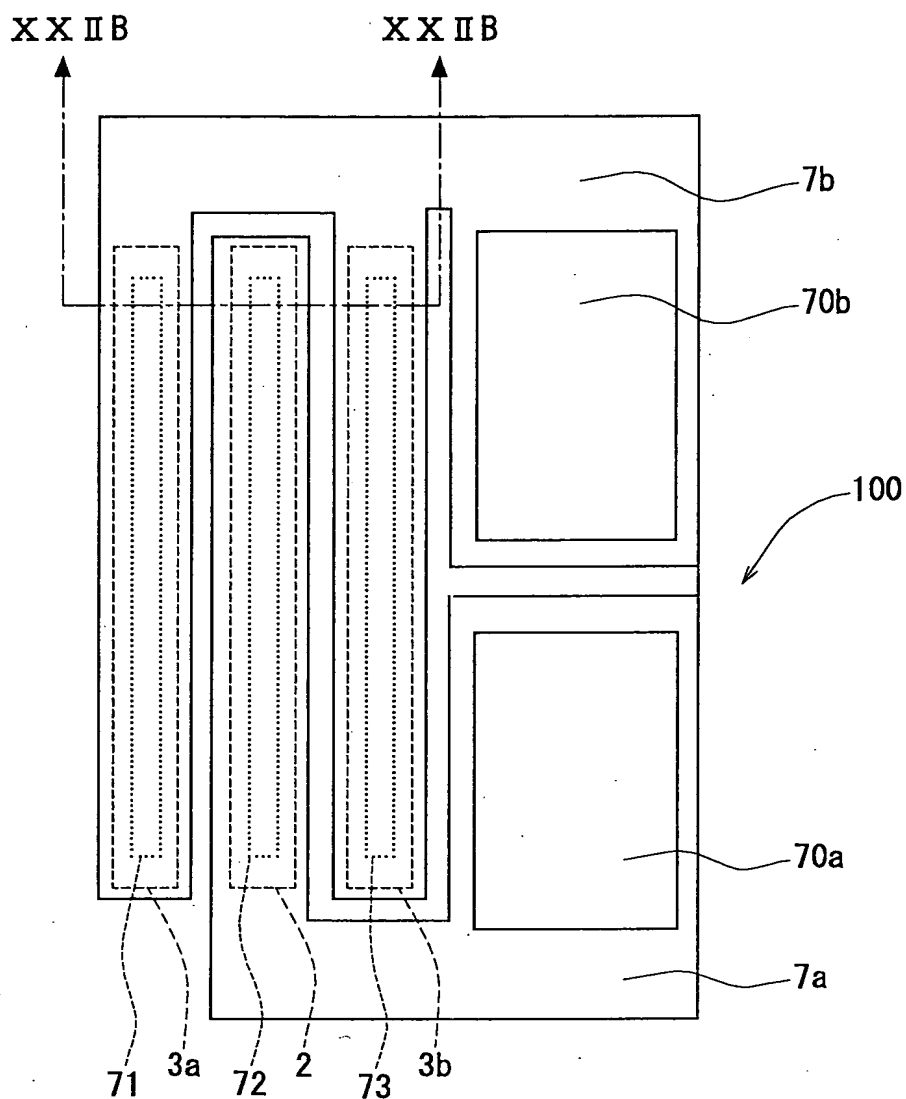


FIG. 22B
RELATED ART

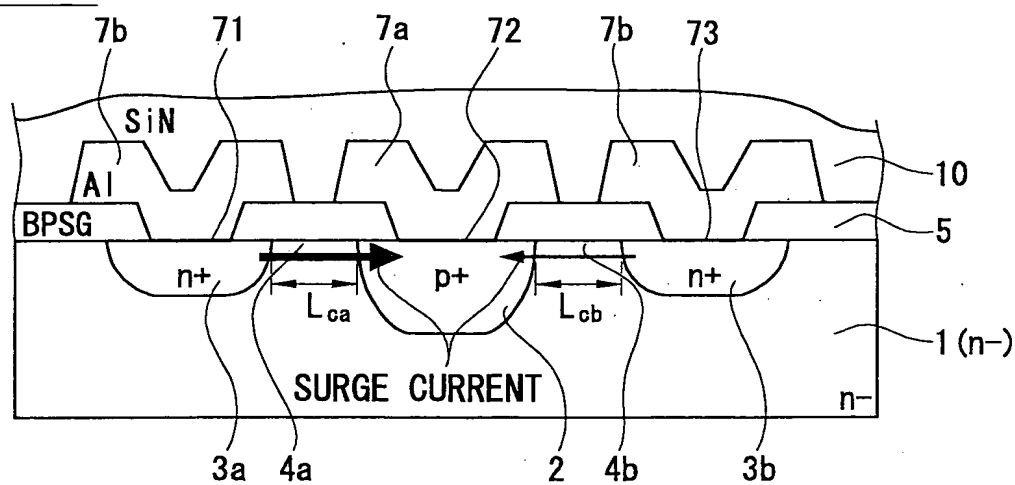


FIG. 23A
RELATED ART

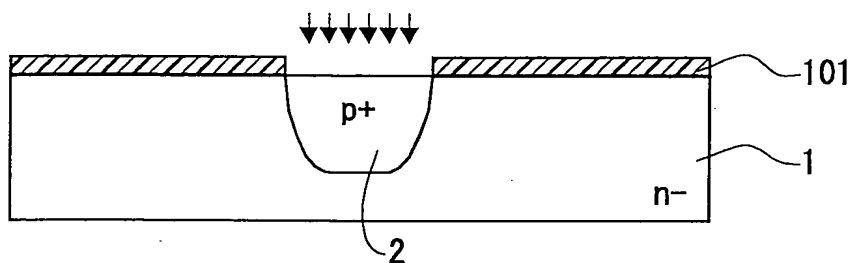


FIG. 23B
RELATED ART

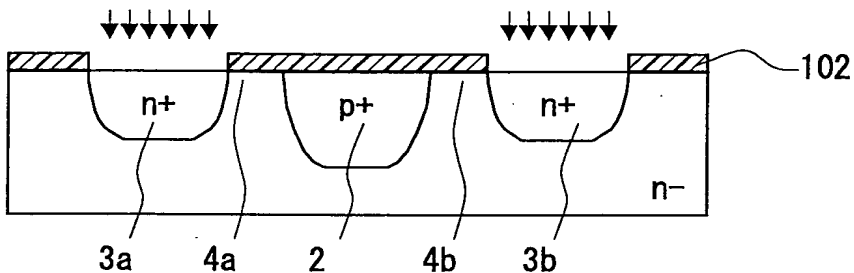


FIG. 23C
RELATED ART

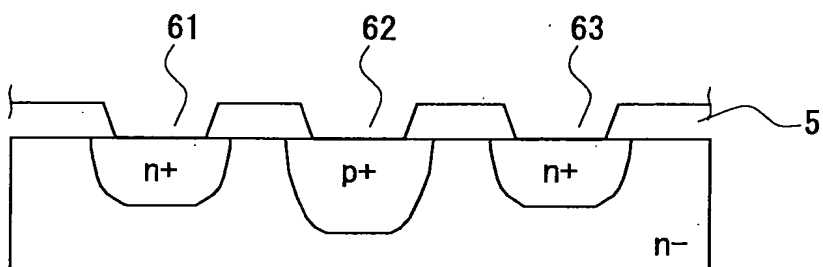


FIG. 23D
RELATED ART

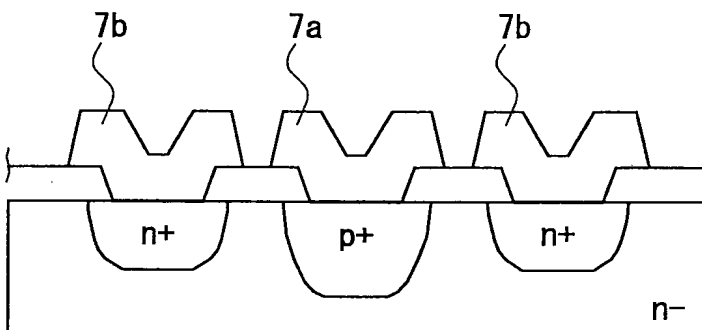


FIG. 23E
RELATED ART

